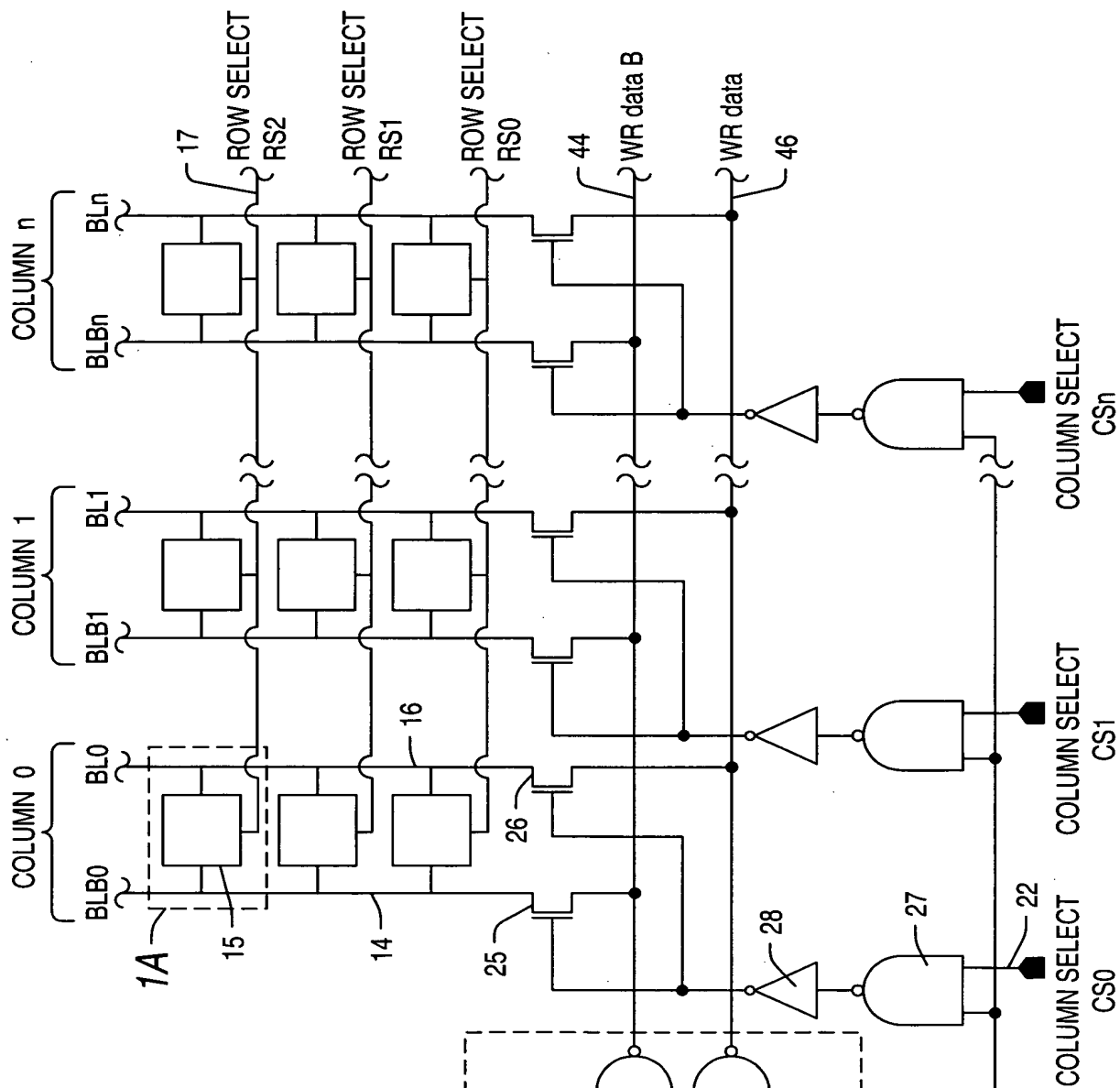


The diagram illustrates a memory array circuit. It features a grid of memory cells defined by row select lines (RS0, RS1, ..., RS_n) and column select lines (CS0, CS1, ..., CS_n). The circuit includes several control inputs: DATA IN, WRITE ENABLE (WE), and WR data B. The output is labeled WR data. The circuit is composed of various logic gates, including AND gates (25, 26, 27, 28, 32, 34), OR gates (29, 30, 31), and inverters (33, 35, 36, 37, 38, 39). The circuit is divided into two main sections: a top section (CIRCUITRY) and a bottom section (CIRCUITRY). The top section contains the main data path and control logic, while the bottom section contains the row and column select logic. The circuit is designed to allow for selective writing and reading of data from the memory array.



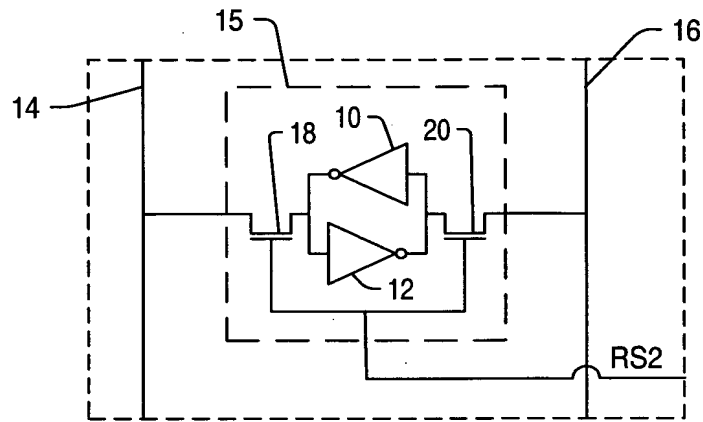


FIG. 1A

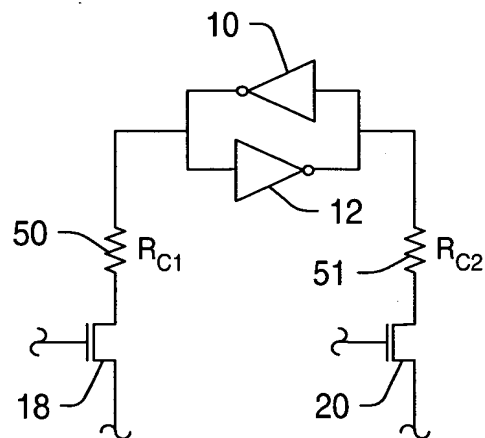


FIG. 2

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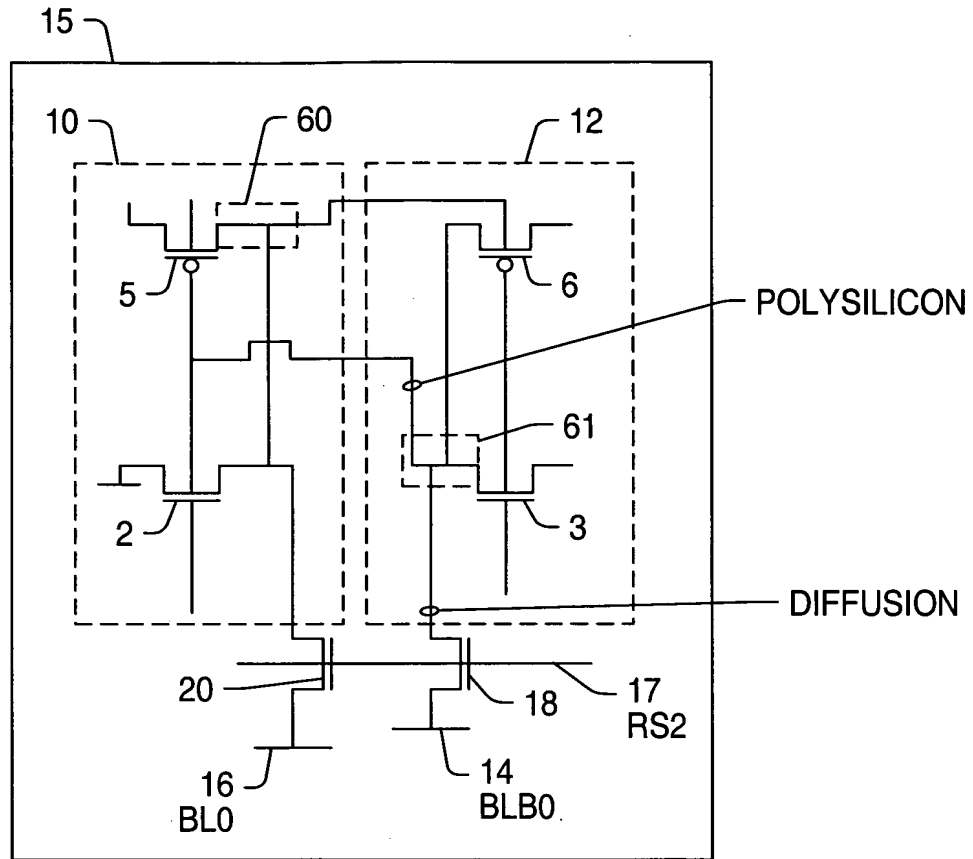


FIG. 3

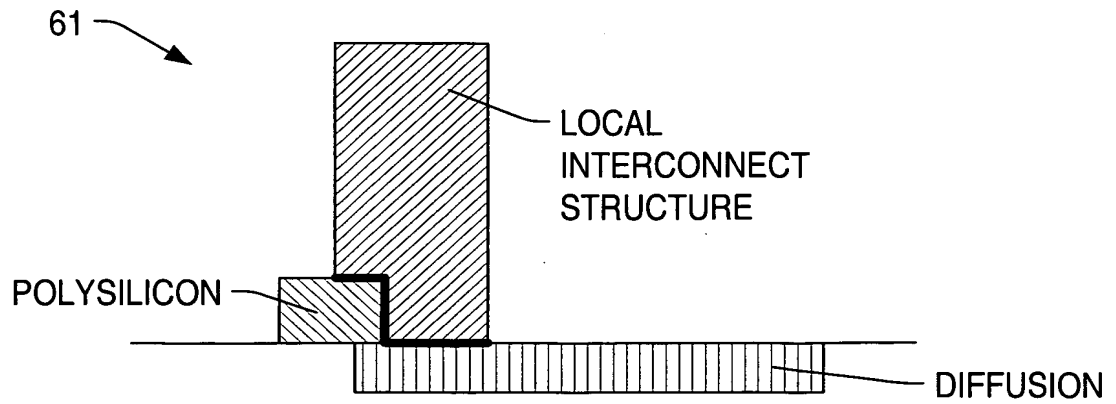


FIG. 3A

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